IN THE CLAIMS

Please amend claims 1, 5, 11, 15, 21, 26 and 28 as indicated below.

Please add new claims 30-50 as indicated below.

1. (Currently Amended) An apparatus, comprising:

a first register to store default configuration data;

a second register coupled to the first register to store active configuration data;

an input circuit coupled to the second register to receive input data different than the default configuration data to be programmed into the second register; and

control logic coupled to the first register, the second register, and the input circuit to load the second register with data selected from either the default configuration data from the first register or input data from the input circuit.

2. (Original) The apparatus of claim 1, further comprising:

reset logic coupled to the first register and the second register, the reset logic to select between loading the second register with the default configuration data and retaining a previous content of the second register in the second register.

3. (Original) The apparatus of claim 2, wherein the reset logic includes:

a first reset line to carry a first reset signal to load default data from the first register into the second register.

4. (Original) The apparatus of claim 3,wherein the first reset line is a power-up reset line.

5. (Currently Amended) The apparatus of claim [[2]] 3, where the reset logic includes:

a programmable selection circuit to store a selection value; and

a second reset line coupled to the programmable selection circuit to carry a second reset signal, [[;]]

wherein a value in the programmable selection circuit is to determine if the second reset signal causes the second register to be loaded with the default configuration data from the first register or causes the second register to retain its data.

6. (Original) The apparatus of claim 5, wherein the second reset line is a warm-start reset line.

7. (Original) The apparatus of claim 1, wherein the input circuit is to receive write data from a data bus, the write data comprising programmable configuration data.

8. (Original) The apparatus of claim 1, wherein the first register is a non-volatile register.

9. (Original) The apparatus of claim 1, wherein the second register is a volatile register.

10. (Original) The apparatus of claim 1, wherein the default configuration data defines a first memory configuration and the programmable configuration data defines a second memory configuration.

11. (Currently Amended A system, comprising:

a processor;

a memory subsystem coupled to the processor and comprising flash memory, the ~~flash~~ memory subsystem including:

a first register to store default configuration data;

a second register coupled to the first register to store active configuration data;

an input circuit coupled to the second register to receive input data different than the default configuration data to be programmed into the second register; and

control logic coupled to the first register, the second register, and the input circuit to load the second register with data selected between the default configuration data from the first register and input data from the input circuit.

12. (Original) The system of claim 11, further comprising:

reset logic coupled to the first register and the second register, the reset logic to select between loading the second register with the default configuration data and retaining a previous content of the second register in the second register.

13. (Original) The system of claim 12, wherein the reset logic includes:

a first reset line to carry a first reset signal to load default data from the first register into the second register.

14. (Original) The system of claim 13,wherein the first reset line is a power-up reset line.

15. (Currently Amended) The system of claim [[12]] 13, where the reset logic includes:

a programmable selection circuit to store a selection value; and

a second reset line coupled to the programmable selection circuit to carry a second reset signal, [[;]]

wherein a value in the programmable selection circuit is to determine if the second reset signal causes the second register to be loaded with the default configuration data from the first register or causes the second register to retain its data.

16. (Original) The system of claim 15, wherein the second reset line is a warm-start reset line.

17. (Original) The system of claim 11, wherein the input circuit is to receive write data from a data bus, the write data comprising programmable configuration data.

18. (Original) The system of claim 11, wherein the first register is a non-volatile register.

19. (Original) The system of claim 11, wherein the second register is a volatile register.

20. (Original) The system of claim 11, wherein the default configuration data defines a first memory configuration and the programmable configuration data defines a second memory configuration.

21. (Currently Amended) A method, comprising:

providing, in a memory device, a first register containing default configuration data;

selecting active configuration data from between the default configuration data in the first register and input data from an input logic circuit, the input logic circuit receiving the input data different than the default configuration data;

writing the active configuration data into a second register; and

using the active configuration data in the second register to specify a configuration.

22. (Original) The method of claim 21, wherein providing the first register includes providing a non-volatile register.

23. (Original) The method of claim 21, wherein writing into the second register includes writing into a volatile register.

24. (Original) The method of claim 21, further comprising:

loading the default configuration data from the first register into the second register upon assertion of a first reset signal.

25. (Original) The method of claim 24, wherein assertion of a first reset signal includes assertion of a power-up reset signal.

26. (Currently Amended) The method of claim [[21]] 24, further comprising:

selecting, upon assertion of a second reset signal, between retaining the active configuration data in the second register and loading the default configuration data from the first register into the second register.

27. (Original) The method of claim 26, wherein assertion of a second reset signal includes assertion of a warm-start reset signal.

28. (Currently Amended) The method of claim [[21]] 26, wherein selecting active configuration data includes selecting programmable configuration data from the input logic circuit to define an operational configuration of a memory that is different than defined by the default configuration data.

29. (Original) The method of claim 21, wherein selecting active configuration data includes selecting default configuration data to define a predetermined intended operational configuration of a memory.

30. (New) The apparatus of claim 3, wherein the input data is programmed into the second register when a write-enable signal is asserted at an enable input of the second register and when the first reset line is de-asserted.

31. (New) The apparatus of claim 5, wherein the second register is programmed with the default configuration data when the second reset line is asserted and the value of the programmable selection circuit has a logical value of one, and wherein the second register is

to the retain previous content when the second reset line is asserted and the value of the programmable selection circuit has a logical value of zero.

32. (New) The apparatus of claim 5, further comprising a first OR gate, wherein the second reset line is coupled to a non-inverted input of the first OR gate and the programmable selection circuit is coupled to an inverted input of the first OR gate, and wherein an output of the first OR gate is used to determine whether the second register is programmed with the default configuration data or the second register is to retain the previous content.

33. (New) The apparatus of claim 32, further comprising an AND gate, wherein the first reset line is coupled to a first input of the AND gate and the output of the first OR gate is coupled to a second input of the AND gate, and wherein an output of the AND gate is used to determine whether the second register is programmed with the default configuration data or the second register is to retain the previous content.

34. (New) The apparatus of claim 33, further comprising:

a second OR gate coupled to the first register and having an output coupled to a set input of the second register; and

a third OR gate coupled to the first register and having an output coupled to a reset input of the second register, the second OR gate setting the second register to a logical value of one and the third OR gate resetting the second register to a logical value of zero.

35. (New) The apparatus of claim 34, wherein the second OR gate comprises an inverted input to receive an output from the first register and a non-inverted input to receive an output from the AND gate.

36. (New) The apparatus of claim 34, wherein the third OR gate comprises a first input to receive an output from the first register and a second input to receive an output from the AND gate.

37. (New) The system of claim 13, wherein the input data is programmed into the second register when a write-enable signal is asserted at an enable input of the second register and when the first reset line is de-asserted.

38. (New) The system of claim 15, wherein the second register is programmed with the default configuration data when the second reset line is asserted and the value of the programmable selection circuit has a logical value of one, and wherein the second register is to the retain previous content when the second reset line is asserted and the value of the programmable selection circuit has a logical value of zero.

39. (New) The system of claim 15, wherein the memory subsystem further comprises a first OR gate, wherein the second reset line is coupled to a non-inverted input of the first OR gate and the programmable selection circuit is coupled to an inverted input of the first OR gate, and wherein an output of the first OR gate is used to determine whether the second register is programmed with the default configuration data or the second register is to retain the previous content.

40. (New) The system of claim 39, wherein the memory subsystem further comprises an AND gate, wherein the first reset line is coupled to a first input of the AND gate and the output of the first OR gate is coupled to a second input of the AND gate, and wherein an output of the AND gate is used to determine whether the second register is programmed with the default configuration data or the second register is to retain the previous content.

41. (New) The system of claim 40, wherein the memory subsystem further comprises:

a second OR gate coupled to the first register and having an output coupled to a set input of the second register; and

a third OR gate coupled to the first register and having an output coupled to a reset input of the second register, the second OR gate setting the second register to a logical value of one and the third OR gate resetting the second register to a logical value of zero.

42. (New) The system of claim 41, wherein the second OR gate comprises an inverted input to receive an output from the first register and a non-inverted input to receive an output from the AND gate.

43. (New) The system of claim 41, wherein the third OR gate comprises a first input to receive an output from the first register and a second input to receive an output from the AND gate.

44. (New) The method of claim 24, wherein the input data is programmed into the second register when a write-enable signal is asserted at an enable input of the second register and when the first reset signal is de-asserted.

45. (New) The method of claim 28, wherein the second register is programmed with the default configuration data when the second reset signal is asserted and the value of the programmable selection circuit has a logical value of one, and wherein the second register is to the retain previous content when the second reset signal is asserted and the value of the programmable selection circuit has a logical value of zero.

46. (New) The method of claim 28, further comprising:

coupling the second reset signal to a non-inverted input of a first OR gate;

coupling the programmable selection circuit to an inverted input of the first OR gate; and

determining whether the second register is programmed with the default configuration data or the second register is to retain the previous content, based on an output of the first OR gate.

47. (New) The method of claim 46, further comprising:

coupling the first reset signal to a first input of an AND gate;

coupling the output of the first OR gate to a second input of the AND gate; and

determining whether the second register is programmed with the default configuration data or the second register is to retain the previous content, based on an output of the AND gate.

48. (New) The method of claim 47, further comprising:

coupling a second OR gate to the first register and having an output coupled to a set input of the second register; and

coupling a third OR gate to the first register and having an output coupled to a reset input of the second register, the second OR gate setting the second register to a logical value of one and the third OR gate resetting the second register to a logical value of zero.

49. (New) The method of claim 48, wherein the second OR gate comprises an inverted input to receive an output from the first register and a non-inverted input to receive an output from the AND gate.

50. (New) The method of claim 48, wherein the third OR gate comprises a first input to receive an output from the first register and a second input to receive an output from the AND gate.